CLAIMS

1. A cellular trench-gate semiconductor device comprising active device cells in a cellular area of a semiconductor body, wherein each active device cell has a channel-accommodating region of a second conductivity type between a surface-adjacent source region and an underlying drain region that are of a first conductivity type, an insulated gate trench accommodating the trench-gate extends from the source region through the channel-accommodating region and into the underlying drain region, the trench-gate being dielectrically coupled to the channel-accommodating region by an intermediate gate dielectric layer at sidewalls of the gate trench, and at least one group of the cells end in a respective end structure including:

- an end region of the second conductivity type having a higher doping concentration than the channel-accommodating region,
- an end trench that is an extension of the insulated gate trench into the end region and that accommodates an extension of the trench-gate,
- and a conductive layer that is connected to the extension of the trench-gate and extends over an intermediate insulating layer over the end region,

which device is characterised in that

- the intermediate insulating layer comprises an area of a trench-etch mask that is of greater thickness than the gate dielectric layer,
- a window extends through the trench-etch mask at a location where the end trench extends into the body and where the conductive layer is connected to the trench-gate extension, and
- the conductive layer has a lateral extent that terminates in an edge on the trench-etch mask.

2. A device according to Claim 1, wherein the respective end structure extends between two groups of active device cells as a stripe structure across a part of the cellular area of the device, the trench-gate, its extension and the conductive layer are of conductive semiconductor material, and a metal track

extends on the conductive semiconductor material on the trench-etch mask to provide a gate connection of reduced electrical resistance for the two groups of active device cells.

3. A device according to Claim 1, wherein the respective end structure extends around a perimeter of the cellular area of the device as a device termination structure, the end region has an outer perimeter that terminates in a field insulator onto which the trench-etch mask extends, and an outwardly-extending field-plate extends over the field insulator over a part of the drain region outside the outer perimeter of the end region and is connected to the trench-gate via the conductive-layer connection.

4. A device according to both Claim 2 and Claim 3, having a first respective end structure that extends around a perimeter of the cellular area as a device termination structure and a second respective end structure that extends as a stripe structure across a part of the cellular area, wherein an area of the field insulator is present under the trench-etch mask under the metal track of the stripe structure.

5. A device according to Claim 2 or 4, wherein the metal track of the stripe structure is insulated by an overlying insulating layer from a source electrode.

6. A device according to Claim 5, wherein an upper metal pattern extends over the overlying insulating layer to provide metal source and gate pads, the metal gate pad contacts the metal track of the stripe structure via a widow in the said overlying insulating layer, and the metal gate pad extends laterally on the said overlying insulating layer over an underlying part of the source electrode.

7. A device according to Claim 3 or Claim 4, wherein an inwardly-extending field-plate is connected to a perimeter region outside an outer perimeter of the field insulator of the device termination structure.

8. A device according to Claim 7, wherein the inwardly-extending field-plate extends over the outer perimeter of the field insulator and onto a further insulating layer over the field insulator of the device termination structure.

9. A device according to any one of Claims 3 to 8, wherein the field insulator comprises deposited material over at least most of its thickness.

10. A device according to any one of Claims 3 to 9, wherein the field insulator of the device termination structure comprises deposited insulating material accommodated within a field trench that is located at the outer perimeter of the respective end region and that extends to a greater depth in the body than the respective end region.

11. A device according to any one of the preceding Claims, wherein the trench-etch mask comprises silicon nitride.

12. A device according to any one of the preceding Claims, wherein the gate dielectric layer comprises a deposited material, an area of which is present on the area of the trench-etch mask below the conductive layer.

13. A device according to any one of the preceding Claims, wherein the conductive layer is an extension of gate material from the end trench onto the insulating layer.

14. A device according to any one of the preceding Claims, wherein both the end trench and gate trench are narrower than the window in the trench-etch mask.

15. A device according to Claim 14, wherein the trench-etch mask has sidewall extensions of a different insulating material at the window so narrowing the window to a width smaller than that of the end trench, the sidewall extensions are more rounded than the adjacent sidewall of the trench-etch mask, and the extension of the trench-gate extends from the end trench over these more rounded sidewall extensions and onto the trench-etch mask.

16. A device according to any one of the preceding Claims, wherein the end trench and gate trench are of the same depth.

17. A device according to any one of the preceding Claims, wherein the end trench extends to a shallower depth than the end region and is accommodated wholly within the end region.

18. A method of manufacturing a cellular trench-gate semiconductor device comprising active device cells in a cellular area of a semiconductor body, each active device cell having a channel-accommodating region of a second conductivity type between a surface-adjacent source region and an underlying drain region that are of a first conductivity type, the trench-gate being accommodated in an insulated gate trench that extends from the source region through the channel-accommodating region and into the underlying drain region, the trench-gate being dielectrically coupled to the channel-accommodating region by an intermediate gate dielectric layer at sidewalls of the gate trench, wherein a respective end structure is provided for at least one group of the cells by process steps that include:

(a) providing in a portion of the drain region adjacent to a surface of the body a surface-adjacent end region of the second conductivity type that has a higher doping concentration than the channel-accommodating region,

(b) providing a trench-etch mask having windows there-through where the gate trench and an end trench are to be etched into the body, the end trench being an extension of the gate trench into the end region,

(c) etching the gate trench and the end trench into the body,

(d) providing the gate dielectric layer at the sidewalls of the gate trench and end trench, the gate dielectric layer having a smaller thickness than the trench-etch mask,

(e) providing gate material in the gate trench and end trench and extending through the windows in the trench-etch mask and onto an upper surface of the trench-etch mask, and

(f) patterning the gate material by etching away areas thereof to leave the gate material

- in the gate trench to form the trench-gate,
- in the end trench and in the associated window to form an extension of the trench-gate,
- and on an adjacent area of the trench-etch mask to form a conductive layer that is connected to the extension of the trench-gate and that has a lateral extent terminating in an edge on the trench-etch mask.

19. A method according to Claim 18, wherein one or more of the additional device features of Claims 2 to 17 are provided.

20. A method according to Claim 18 or 19, wherein, after patterning the gate material in step (f), the trench-etch mask and its windows are used to provide the source region and/or an insulating capping layer on the trench-gate in a self-aligned manner with respect to the gate trench.

21. A method according to any one of Claims 18 to 20, wherein the trench-etch mask comprises silicon nitride that is provided in step (b) over at least a major area of a field-oxide and that protects this field-oxide area during subsequent processing steps such as the steps (c) and (f).

22. A method according to any one of Claims 18 to 21, wherein the trench-etch mask comprises silicon nitride that is provided in step (b), an oxide

layer is provided after step (f) over the nitride area of the trench-etch mask in the end structure, and this oxide layer protects the underlying nitride area when the trench-etch mask is subsequently etched away from the active device cells.